AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph that begins on page 7 and continues onto page 8 to read as follows:

--Delay 41 also generates an address enable signal ADD_EA by delaying the primary index enable signal IN_EA1 for a time T2. Time T2 is longer than the time T1 of the comparator enable signal COMP_EA, but less than time T, the period of the primary index enable signal IN_EA1 (i.e., T1<T2<T). Delay 41 transmits the address enable signal ADD_EA to the address generator 44. When address generator 44 receives the address enable signal ADD_EA, the address generator 44 converts the index I received from the index generator 43 to a read address for the memory 45. Memory 45 then outputs the data stored in that address. Index I at the input of the address generator 44, at the time the address enable signal ADD_EA is received, is either that index generated by the primary index enable signal IN_EA1 or the next index I generated by the secondary index enable signal IN_EA2, if so generated by comparator 42. If the index I generated at the primary index enable time is less than the input data size S, the index I is converted to a read address by address generator 44. If the generated index is greater than the input data size S ~~two-dimensional matrix size K~~, the next index, generated in response to the secondary index enable signal IN_EA2 output from the comparator 42, is converted to a read address by address generator 44. Since the comparator enable signal COMP_EA and the address enable signal ADD_EA are generated before the next primary index enable signal IN_EA1, read addresses are successively generated without time delay.--